

SANYO

No.4457

LC66562B, 66566B**12 and 16-kbyte on-chip ROM capacities
CMOS 4-bit single-chip microcontrollers**

Overview

The LC66562B and 66566B are CMOS 4-bit microcontrollers that integrate in a single chip all the functionality required for control applications, including ROM, RAM, I/O ports, serial interfaces, comparator inputs, three-value inputs, timers, and interrupt functions. The LC66562B and 66566B are provided in LC66566A series.

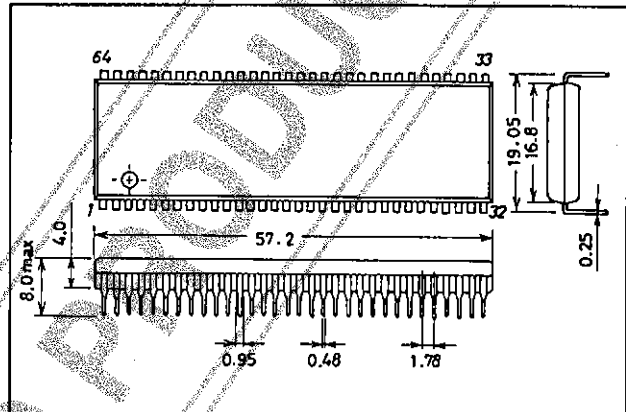
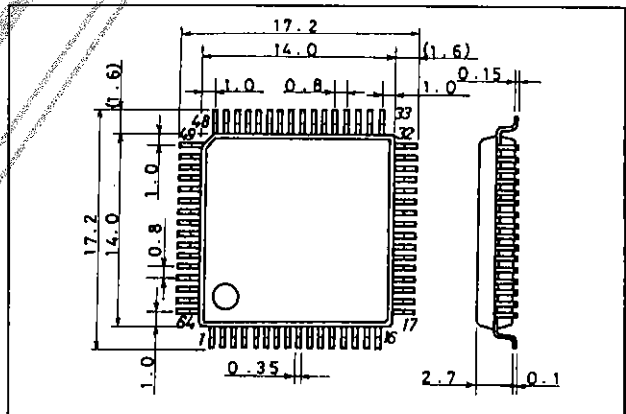
The LC66562B and 66566B differ from the earlier LC66566A series in the power supply voltage range and certain other electrical specifications.

Features and Functions

- A 12- or 16-kbyte on-chip ROM capacity, and an on-chip RAM capacity of 512 by 4 bits
- Support for the full 128 instruction LC66000 series instruction set
- Fifty four I/O ports
- Two 8-bit serial interfaces (that can be connected in a 16-bit cascade format)
- Instruction cycle: 0.92 to 10 μ s (3 to 5.5 V)
- Powerful timer and prescaler functions
 - 12-bit timer based time limit timer, event counter, pulse width measurement, and square wave output functions
 - 8-bit timer based time limit timer, event counter, PWM output, and square wave output functions
 - 12-bit prescaler based time base function
- Powerful 11-factor 8-vector interrupt system
 - External interrupts: 6 factors, 3 vectors
 - Internal interrupts: 5 factors, 5 vectors
- Flexible I/O functions
 - Comparator inputs, three-value inputs, 20 mA drive outputs, 15 V breakdown voltage, pull-up/open drain option switching
- Runaway detection function (watchdog timer) option
- 8-bit I/O functions
- Low power functions using halt and hold modes
- Packages: DIP64S, QFP64E
- Test and evaluation ICs: LC66599 (evaluation chip) + EVA850/800-TB665xx
LC66E516 (built-in EPROM microcontroller)
LC66P516 (built-in OTPROM microcontroller)

Package Dimensions

unit: mm

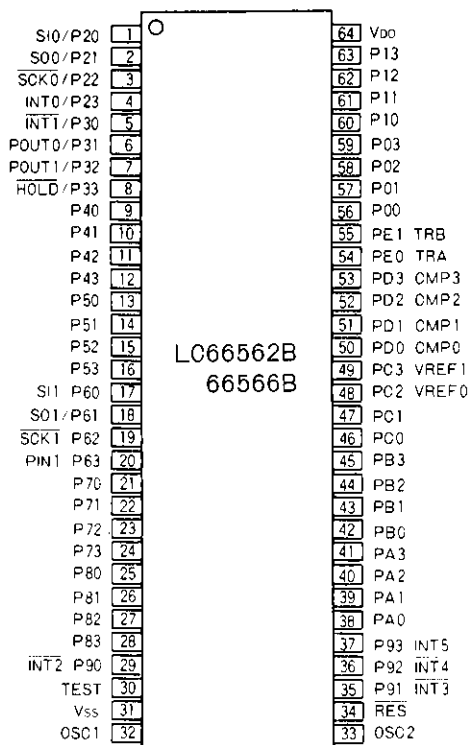
3071-DIP64S**3159-QFP64E****SANYO Electric Co., Ltd. Semiconductor Business Headquarters**

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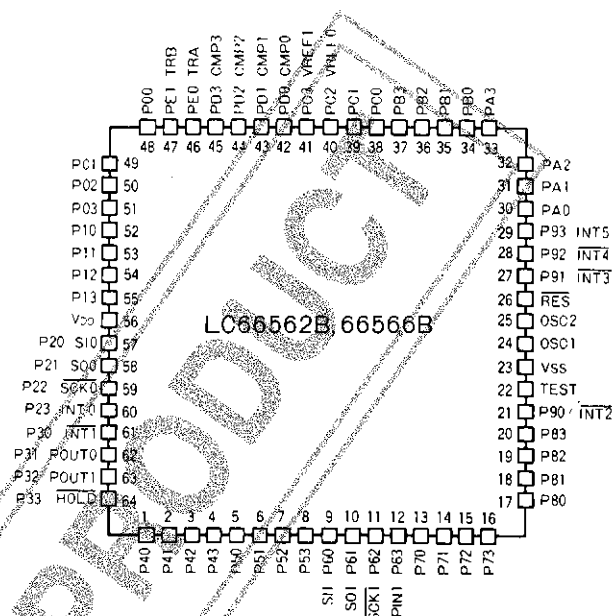
Pin Assignment

DIP64S

QFP64E



Top View

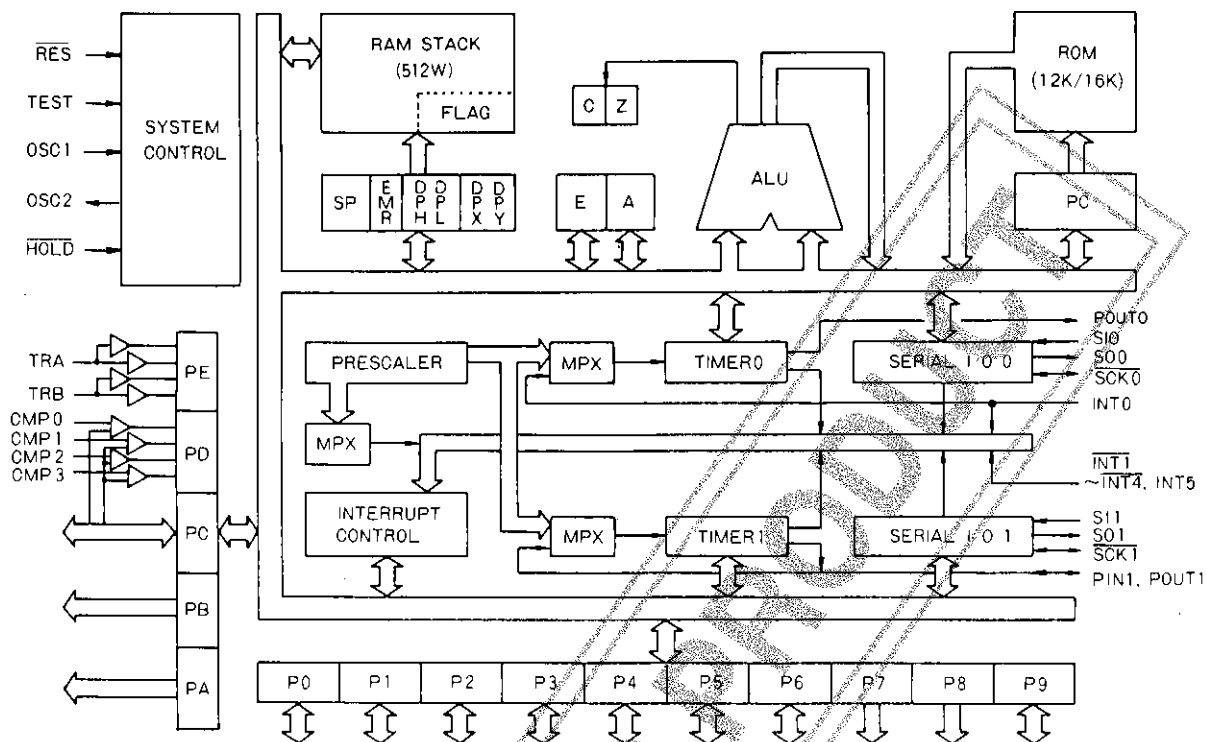


Series Organization

Product no.	Pin count	ROM capacity	RAM capacity	Package	Features
LC66304A/306A/308A	42	4 k/6 k/8 kB	512 W	DIP42S QFP48E	Normal version
LC66404A/406A/408A	42	4 k/6 k/8 kB	512 W	DIP42S QFP48E	4.0 to 6.0 V/0.92 μs
LC66506B/508B/512B/516B	64	6 k/8 k/12 k/16 kB	512 W	DIP64S QFP64A	Low voltage version 2.2 to 5.5 V/3.92 μs
LC66354A/356A/358A	42	4 k/6 k/8 kB	512 W	DIP42S QFP48E	
LC66354S/356S/358S*	42	4 k/6 k/8 kB	512 W	QFP44M	Low voltage high speed version 3.0 to 5.5 V/0.92 μs
LC66556A/558A/562A/566A	64	6 k/8 k/12 k/16 kB	512 W	DIP64S QFP64E	
LC66354B/356B/358B*	42	4 k/6 k/8 kB	512 W	DIP42S QFP48E	Window and OTP versions for testing and evaluation 4.5 to 5.5 V/0.92 μs
LC66556B/558B*	64	6 k/8 k	512 W	DIP64S QFP64E	
LC66562B/566B	64	12 k/16 kB	512 W	DIP64S QFP64E	
LC66E308	42	EPROM 8 kB	512 W	DIC42S (window) QFC48 (window)	
LC66P308	42	OTPROM 8 kB	512 W	DIP42S QFP48E	
LC66E408	42	EPROM 8 kB	512 W	DIC42S (window) QFC48 (window)	
LC66P408	42	OTPROM 8 kB	512 W	DIP42S QFP48E	
LC66E516	64	EPROM 16 kB	512 W	DIC64S (window) QFC64 (window)	
LC66P516	64	OTPROM 16 kB	512 W	DIP64S QFP64E	

Note: * Products market with an asterisk are under development.

System Block Diagram



Differences between the LC66562B/LC66566B and the LC66516B Series

Parameter	LC66516B series (including the EVA850/800-TB665XX tools)	LC66562B, 66566B
System level differences	65536 cycles: About 64 ms at 4 MHz (T _{cyc} = 1 μs)	16384 cycles: About 16 ms at 4 MHz (T _{cyc} = 1 μs)
• Hardware waiting time for clearing hold mode		
• The timer 0 value on reset (including the value after clearing hold mode)	The value FF0 is loaded	The value FFC is loaded
Feature differences	LC66512B, 516B 4.0 to 6.0 V/0.92 to 10 μs	3.0 to 5.5 V/0.92 to 10 μs
• Operating power supply voltage/operating speed	LC66E516, P516 4.5 to 5.5 V/0.92 to 10 μs	

- An RC oscillator cannot be used with the LC66562B and LC66566B
- In addition there are differences in output currents and comparator input voltages. For details, refer to the LC66516B, LC66E516, and LC66P516 catalogs. Special care should be exercised with respect to these differences when using the LC66E516, and LC66P516 evaluation products.

DISCONTINUED

Pin Description

Pin	I/O	Function	Output driver type	Options	Value on reset
P00 P01 P02 P03	I/O	I/O ports P00 to P03 • Input and output in 1 or 4 bit units • P00 to P03 have halt mode control functions	Pch: Pu MOS type Nch: Low sink current type	• Pu MOS attached or Nch OD output • Output level on reset	High or low (option)
P10 P11 P12 P13	I/O	I/O ports P10 to P13 • Input and output in 1 or 4 bit units	Pch: Pu MOS type Nch: Low sink current type	• Pu MOS attached or Nch OD output • Output level on reset	High or low (option)
P20/SI0 P21/SO0 P22/SCK0 P23/INT0	I/O	I/O ports P20 to P23 • Input and output in 1 or 4 bit units • P20 is also used as the serial input SI0. P21 is also used as the serial output SO0. P22 is also used as the serial clock SCK0. • P23 is also used as the INT0 interrupt request, the timer 0 event count, and the pulse width measurement inputs	Pch: CMOS type Nch: Low sink current type Breakdown voltage of +15 V on Nch OD	• CMOS or Nch OD output	High
P30/INT1 P31/POUT0 P32/POUT1	I/O	I/O ports P30 to P32 • Input and output in 1 or 3 bit units • P30 is also used as the INT1 interrupt request • P31 is also used as the square wave output from timer 0 • P32 is also used as the square wave output and PWM output from timer 1	Pch: CMOS type Nch: Low sink current type Breakdown voltage of +15 V on Nch OD	• CMOS or Nch OD output	High
P33/HOLD	I	Hold mode control input • Hold mode is set by a HOLD instruction when $\overline{\text{HOLD}}$ is low • In hold mode the CPU is restarted by setting the $\overline{\text{HOLD}}$ input high • This pin can be used as input port P33 along with P30 to P32 • When the P33/ $\overline{\text{HOLD}}$ pin is low, the CPU will not be reset by a low level on $\overline{\text{RES}}$. Therefore, applications must not hold the P33/ $\overline{\text{HOLD}}$ pin low when power is first applied.			
P40 P41 P42 P43	I/O	I/O ports P40 to P43 • Input and output in 1 or 4 bit units • Input and output in 8 bit units when used in conjunction with P50 to P53. • ROM data output in 8 bit units when used in conjunction with P50 to P53	Pch: Pu MOS type Nch: Low sink current type	• Pu MOS attached or Nch OD output	High
P50 P51 P52 P53	I/O	I/O ports P50 to P53 • Input and output in 1 or 4 bit units • Input and output in 8 bit units when used in conjunction with P40 to P43. • ROM data output in 8 bit units when used in conjunction with P40 to P43	Pch: Pu MOS type Nch: Low sink current type	• Pu MOS attached or Nch OD output	High
P60/SI1 P61/SO1 P62/SCK1 P63/PIN1	I/O	I/O ports P60 to P63 • Input and output in 1 or 4 bit units • P60 is also used as the serial input SI1. P61 is also used as the serial output SO1 • P62 is also used as the serial clock SCK1 • P63 is also used as the event count input to timer 1	Pch: CMOS type Nch: Low sink current type Breakdown voltage of +15 V on Nch OD	• CMOS or Nch OD output	High

Notes: PU MOS attached: Output pins with a pull-up MOS transistor
 CMOS output: Complementary output
 OD output: Open drain output

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Pin	I/O	Function	Output driver type	Options	Value on reset
P70 P71 P72 P73	O	Output only ports P70 to P73 • Output in 1 or 4 bit units • The latched output values are read in by input instructions	Pch: Pu MOS type Nch: Low sink current type Breakdown voltage of +15 V on Nch OD	• Pu MOS attached or Nch OD output	High
P80 P81 P82 P83	O	Output only ports P80 to P83 • Output in 1 or 4 bit units • The latched output values are read in by input instructions • Pch OD output option available	Pch: CMOS type Nch: Low sink current type	• CMOS or Pch OD output • Output level on reset	High or low (option)
P90/INT2 P91/INT3 P92/INT4 P93/INT5	I/O	I/O ports P90 to P93 • Input and output in 1 or 4 bit units • P90 is also used as the INT2 interrupt request • P91 is also used as the INT3 interrupt request • P92 is also used as the INT4 interrupt request • P93 is also used as the INT5 interrupt request	Pch: CMOS type Nch: Low sink current type	• CMOS or Nch OD output	High
PA0 PA1 PA2 PA3	O	Output only ports PA0 to PA3 • Output in 1 or 4 bit units • The latched output values are read in by input instructions	Pch: Pu MOS type Nch: Low sink current type Breakdown voltage of +15 V on Nch OD	• Pu MOS attached or Nch OD output	High
PB0 PB1 PB2 PB3	O	Output only ports PB0 to PB3 • Output in 1 or 4 bit units • The latched output values are read in by input instructions	Pch: Pu MOS type Nch: Low sink current type	• Pu MOS attached or Nch OD output	High
PC0 PC1 PC2/VREF0 PC3/VREF1	I/O	I/O ports PC0 to PC3 • Input and output in 1 or 4 bit units • PC2 is also used as the VREF0 comparator comparison voltage pin • PC3 is also used as the VREF1 comparator comparison voltage pin	Pch: CMOS type Nch: Low sink current type	• CMOS or Nch OD output	High
PD0/CMP0 PD1/CMP1 PD2/CMP2 PD3/CMP3	I	Input only ports PD0 to PD3 • Can be switched in software to function as comparator inputs. The PD0 comparison voltage is VREF0. The PD1 to PD3 comparison voltage is VREF1. Comparators are specified in units of PD0, PD1 (PD2, PD3).			Normal input
PE0/TRA PE1/TRB	I	Input only ports • Can be switched in software to function as three value input ports			Normal input
OSC1 OSC2	I O	System clock oscillator pins. When an external clock is used, leave OSC2 open and input the clock signal to OSC1		• Selection of ceramic oscillator or external clock	
RES	I	System reset input pin • The CPU is initialized when P33/HOLD is high and RES is set to low			
TEST	I	CPU test pin. Always connect this pin to V _{SS} during normal operation.			
V _{DD} V _{SS}		Power supply pins			

Notes: PU MOS attached: Output pins with a pull-up MOS transistor
 CMOS output: Complementary output
 OD output: Open drain output

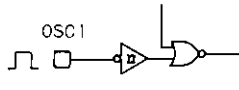
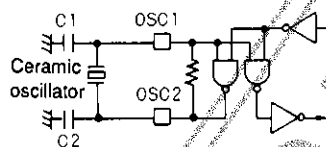
User Options

1. Ports 0, 1, and 8 output level on reset option

The output levels for the I/O ports 0, 1, and 8 in 4-bit sets can selected to be either of the following two option.

Option	Conditions
High level output after reset	The 4 bits of each of ports 0, 1, and 8 as a set
Low level output after reset	The 4 bits of each of ports 0, 1, and 8 as a set

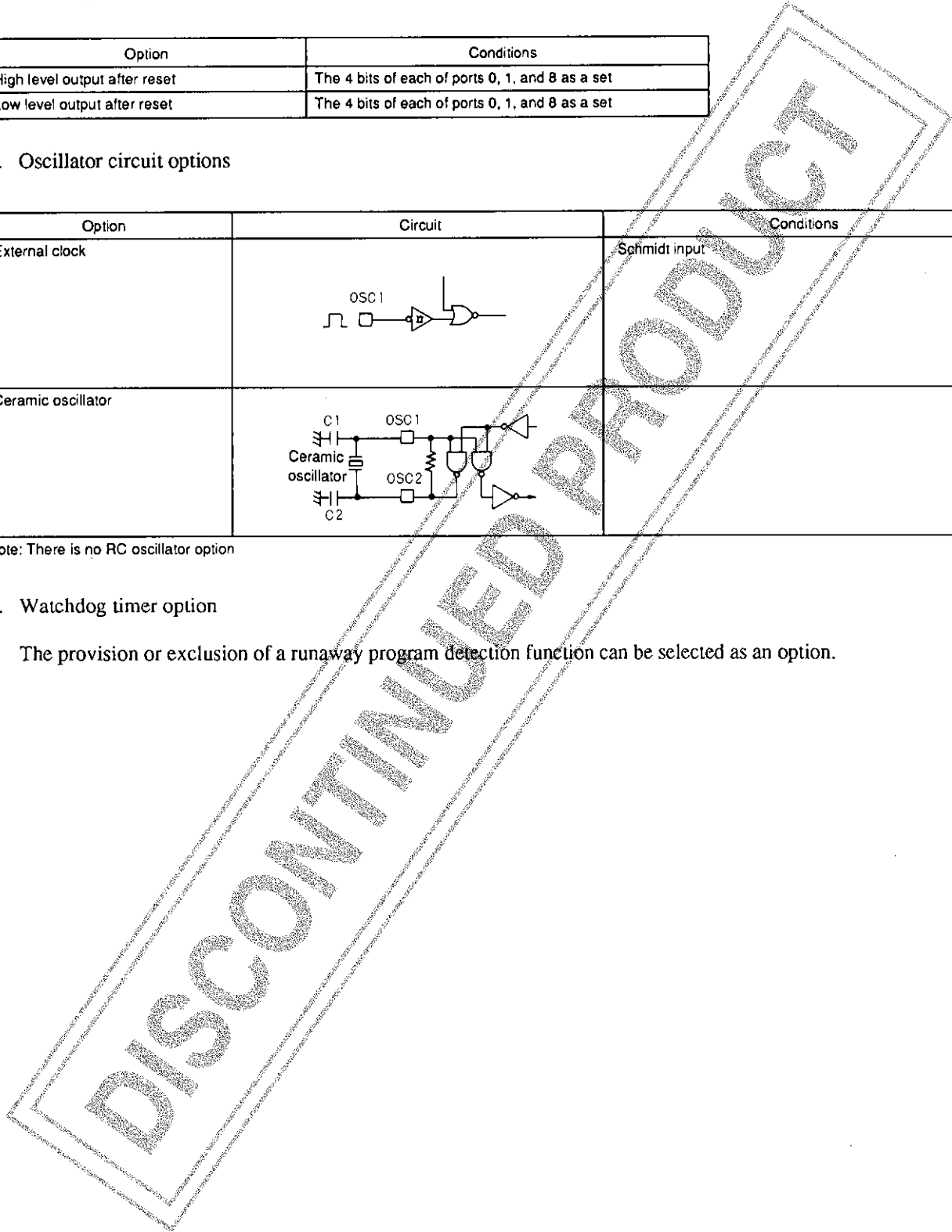
2. Oscillator circuit options

Option	Circuit	Conditions
External clock		Schmidt input
Ceramic oscillator		

Note: There is no RC oscillator option

3. Watchdog timer option

The provision or exclusion of a runaway program detection function can be selected as an option.



4. Port output format option

- The following two options are available in bit units for each of the ports P0, P1, P2, P3 (except for P33/HOLD), P4, P5, P6, P7, P9, PA, PB, and PC.

Option	Circuit	Conditions
Open drain output		P7, PA, and PB are output only. P2, P3, P6, and P9 are schmidt inputs.
Pull-up resistor output		P7, PA, and PB are output only. P2, P3, P6, and P9 are schmidt inputs. The CMOS output (P2, P3, P6, P9, and PC) and the P _u MOS outputs (P0, P1, P4, P5, P7, PA, and PB) are differentiated by the Pch Tr's drive ability.

- The following two options can be available in bit units for P8.

Option	Circuit	Conditions
Open drain output		
Pull-down resistor output		

- The PD comparator inputs and the PE three value inputs are selected in software.

DISCONTINUED PRODUCT

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Applicable pins, notes	Conditions	Rated value	Unit	Notes
Maximum power supply voltage	$V_{DD\text{ max}}$	V_{DD}		-0.3 to +7.0	V	
Input voltages	$V_{IN(1)}$	P2, P3 (except for P33/HOLD), P6		-0.3 to +15.0	V	1
	$V_{IN(2)}$	Other inputs		-0.3 to $V_{DD} + 0.3$	V	2
Output voltages	$V_{OUT(1)}$	P2, P3 (except for P33/HOLD), P6, P7, PA		-0.3 to +15.0	V	1
	$V_{OUT(2)}$	Other outputs		-0.3 to $V_{DD} + 0.3$	V	2
Output current per pin	$I_{ON(1)}$	P0, P1, P2, P3 (except for P33/HOLD), P4, P5, P6, P8, P9, PC		4	mA	3
	$I_{ON(2)}$	P7, PA, PB		20	mA	3
	$-I_{OP(1)}$	P0, P1, P4, P5, P7, PA, PB		2	mA	4
	$-I_{OP(2)}$	P2, P3 (except for P33/HOLD), P6, P8, P9, PC		4	mA	4
Total pin current	$\Sigma I_{ON(1)}$	P2, P3 (except for P33/HOLD), P4, P5, P6, P7, P8		75	mA	3
	$\Sigma I_{ON(2)}$	P0, P1, P9, PA, PB, PC		75	mA	3
	$-\Sigma I_{OP(1)}$	P2, P3 (except for P33/HOLD), P4, P5, P6, P7, P8		25	mA	4
	$-\Sigma I_{OP(2)}$	P0, P1, P9, PA, PB, PC		25	mA	4
Maximum power dissipation	$P_d\text{ max}$	$T_a = -30\text{ to }+70^\circ\text{C}$	DIP64S (QFP64E)	600 (430)	mW	5
Operating temperature range	T_{opr}			-30 to +70	$^\circ\text{C}$	
Storage temperature range	T_{sig}			-55 to +125	$^\circ\text{C}$	

Notes: 1. Applies to open drain output specification pins. For output specifications other than open drain, the ratings in other pin items apply.

2. For oscillator input and output, up to the free running oscillation frequency is allowed.

3. Input current (For pin P8, applies to the CMOS output specifications.)

4. Output current (For pins other than P8, applies to the pull-up output and to the CMOS output specifications.)

5. We recommend reflow soldering as the soldering method for QFP packages.

Please contact your Sanyo sales or technical representative for the conditions required for the use of methods in which the package itself is directly immersed in a solder dip bath.

DISCONTINUED

Allowable Operating Ranges, Unless Otherwise Specified at Ta = -30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V

Parameter	Symbol	Applicable pins	Conditions	Ratings			Unit	Notes	
				V _{DD} (V)	min	typ			max
Operating power supply voltage	V _{DD}	V _{DD}			3.0		5.5	V	
Memory retention power supply voltage	V _{DD(H)}	V _{DD}	During hold mode		1.8		5.5	V	
Input high level voltage	V _{IH(1)}	P2, P3 (except for P33/HOLD), P6	With the output Nch Tr off		0.8 V _{DD}		13.5	V	1
	V _{IH(2)}	P33/HOLD, P9 RES, OSC1	With the output Nch Tr off		0.8 V _{DD}		V _{DD}	V	2
	V _{IH(3)}	P0, P1, P4, P5, PC, PD, PE	With the output Nch Tr off		0.75 V _{DD}		V _{DD}	V	3
	V _{IH(4)}	PE	When three value inputs are used		0.8 V _{DD}		V _{DD}	V	
Intermediate level input voltage	V _{IM}	PE	When three value input used		0.4 V _{DD}		0.6 V _{DD}	V	
Common mode input voltage rage	V _{CMM(1)}	PD0, PC2	When comparator input used		1.5		V _{DD}	V	
	V _{CMM(2)}	PD1, PD2, PD3, PC3			V _{SS}		V _{DD} - 1.5		
Input low level voltage	V _{IL(1)}	P2, P3 (except for P33/HOLD), P6, P9, RES, OSC1	Output Nch Tr off		V _{SS}		0.2 V _{DD}	V	2
	V _{IL(2)}	P33/HOLD		1.8 to 5.5	V _{SS}		0.2 V _{DD}	V	
	V _{IL(3)}	P0, P1, P4, P5, PC, PD, PE, TEST	Output Nch Tr off		V _{SS}		0.25 V _{DD}	V	3
	V _{IL(4)}	PE	When three value input used		V _{SS}		0.2 V _{DD}	V	
Operating frequency	f _{op} (T _{cyc})				0.4 (10)		4.35 (0.92)	MHz (μs)	
External clock input conditions	Frequency	f _{ext}	OSC1 According to figure 1 Clock input to OSC1, OSC2 left open (When the external clock input option is selected as the oscillator circuit.)		0.4		4.35	MHz	
	Pulse width	t _{extH} t _{extL}			100			ns	
	Rise and fall time	t _{extR} t _{extF}						30	ns

- Notes: 1. Applies to the open drain specification pins. However, V_{IH(2)} applies to P33/HOLD.
 2. Applies to the open drain specification pins. The CMOS output specification P9 cannot be used for input.
 3. When PE is used for three value input, V_{IH(4)}, V_{IM}, and V_{IL(4)} apply. The CMOS output specification PC cannot be used for input.

DISCONTINUED

Electrical characteristics, Unless Otherwise Specified at Ta = -30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V

Parameter	Symbol	Applicable Pins	Conditions	Ratings			Unit	Notes	
				V _{DD} (V)	min	typ			max
Input high level current	I _{IH} (1)	P2, P3 (except for P33/HOLD), P6	V _{IN} = 13.5 V, output Nch Tr off				5.0	μA	1
	I _{IH} (2)	P0, P1, P4, P5, P9, PC, OSC1, RES, P33/HOLD (except for PD, PE, PC2, and PC3)	V _{IN} = V _{DD} , output Nch Tr off				1.0	μA	1
	I _{IH} (3)	PD, PE, PC2, PC3	V _{IN} = V _{DD} , output Nch Tr off				1.0	μA	1
Input low level current	I _{IL} (1)	Inputs other than PD, PE, PC2, and PC3	V _{IN} = V _{SS} , output Nch Tr off		-1.0			μA	2
	I _{IL} (2)	PC2, PC3, PD, PE	V _{IN} = V _{SS} , output Nch Tr off		-1.0			μA	2
Output high level current	V _{OH} (1)	P2, P3 (except for P33/HOLD), P6, P8, P9, PC	I _{OH} = -1 mA I _{OH} = -0.1 mA		V _{DD} - 1.0 V _{DD} - 0.5			V	3
	V _{OH} (2)	P0, P1, P4, P5, P7, PA, PB	I _{OH} = -50 μA I _{OH} = -30 μA		V _{DD} - 1.0 V _{DD} - 0.5			V	4
Output pull-up current	I _{PO}	P0, P1, P4, P5, P7, PA, PB	V _{IN} = V _{SS}	5.5	-1.6			mA	4
Output low level current	V _{OL} (1)	P0, P1, P2, P3, P4, P5, P6, P8, P9, PC (except for P33/HOLD)	I _{OL} = 1.6 mA				0.4	V	5
	V _{OL} (2)	P7, PA, PB	I _{OL} = 8 mA				1.5	V	
Output off leakage current	I _{OFF} (1)	P2, P3, P6, P7, PA	V _{IN} = 3.5 V				5.0	μA	6
	I _{OFF} (2)	(Except for P2, P3, P6, P7, P8, and PA)	V _{IN} = V _{DD}				1.0	μA	6
	I _{OFF} (3)	P8	V _{IN} = V _{SS}		-1.0			μA	7
Comparator offset voltage	V _{OFF} (1)	PD1, PD2, PD3	V _{IN} = V _{SS} to V _{DD} - 1.5 V			±50	±300	mV	
	V _{OFF} (2)	PD0	V _{IN} = 1.5 V to V _{DD}			±50	±300	mV	
Schmitt characteristics	Hysteresis voltage	V _{HIS}	P2, P3, RES, P6, P9, OSC1 (RC, EXT)			0.1 V _{DD}		V	
	High level threshold voltage	V _{IH}			0.5 V _{DD}		0.8 V _{DD}	V	
	Low level threshold voltage	V _{IL}			0.2 V _{DD}		0.5 V _{DD}	V	
Ceramic oscillator	Oscillator frequency	f _{CF}	OSC1, OSC2	According to figure 2	4 MHz		4.0		MHz
	Oscillator stabilization time	t _{CBS}		According to figure 3	4 MHz			10	ms

- Notes: 1. For shared I/O ports, open drain output specifications, this applies when the output Nch Tr is off. Cannot be used as input pins under the CMOS specifications.
2. For shared I/O ports with open drain output specifications, this applies when the output Nch Tr is off. Pull-up output specification ratings are stipulated for the output current IPO. Cannot be used as input pins under the CMOS specifications.
3. Under the CMOS output specifications, this applies when the output Nch Tr is off. (Also applies to P8 open drain.)
4. Under the pull-up output specifications, this applies when the output Nch Tr is off.
5. For P8, this applies for the CMOS output specifications.
6. Under the open drain output specifications, this applies when the output Nch Tr is off.
7. Under the open drain output specifications, this applies when the output Pch Tr is off.

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Parameter		Symbol	Applicable Pins		Conditions	Ratings			Unit	Notes	
						V _{DD} (V)	min	typ			max
Serial clock	Cycle timer	Input	t _{CKCY}	SCK0, SCK1	With the timing of figure 4 and the test load of figure 5		0.9			μs	
		Output					2.0			T _{cyc}	
	Low level and high level pulse width	Input	t _{CKL}				0.4			μs	
		Output	t _{CKH}				1.0			T _{cyc}	
Rise and fall time	Output	t _{CKR} t _{CKF}			0.1	μs					
Serial input	Data setup time	t _{ICK}	S10, S11 S10, S11	With the timing of figure 4. Stipulated with respect to the rise of SCK0 and SCK1.			0.3			μs	
	Data hold time	t _{CKI}					0.3			μs	
Serial output	Output delay time	t _{CKO}	SO0, SO1	With the timing of figure 4 and the test load of figure 5. Stipulated with respect to the fall of SCK0 and SCK1.				0.3	μs		
Pulse input conditions	INT0 high and low level pulse width	t _{I0H} t _{I0L}	INT0	Figure 6 • Conditions such that an INT0 interrupt will be accepted • Conditions such that counter/timer 0 event or pulse width measurement input will be accepted			2			T _{cyc}	
	Interrupt input high and low level pulse width other than INT0	t _{I1H} t _{I1L}	INT1, INT2, INT3, INT4, INT5				• Conditions such that each interrupt will be accepted	2			T _{cyc}
	PIN1 high and low level pulse width	t _{P1NH} t _{P1NL}	PIN1				• Conditions such that a timer 1 event counter input will be accepted	2			T _{cyc}
	RES high and low level pulse width	t _{RSH} t _{RSL}	RES				• Conditions such that a reset occurs	3			T _{cyc}
Comparator response time	T _{RS}	PD	Figure 7					20	ms		
Operating mode quiescent current	I _{DD OP}	V _{DD}					4 MHz ceramic oscillator	3.0	5.0	mA	1
							4 MHz external clock	3.0	5.0	mA	
Halt mode quiescent current	I _{DD HALT}	V _{DD}					4 MHz ceramic oscillator	1.0	2.0	mA	
							4 MHz external clock	1.0	2.0	mA	
Hold mode quiescent current	I _{DD HOLD}	V _{DD}					1.8 to 5.5	0.01	10	μA	

Note: 1. Reset state.

DISCONTINUED PRODUCT

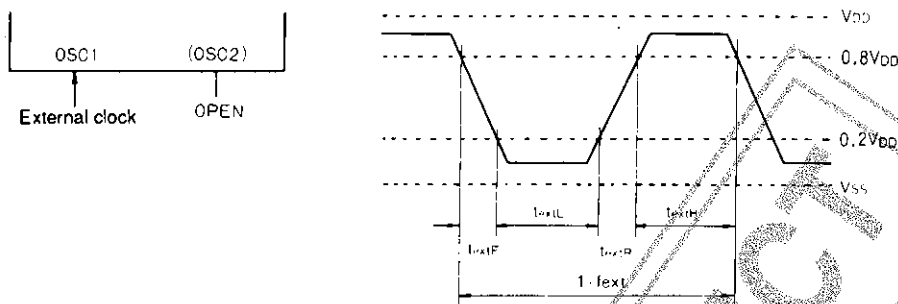


Figure 1: External Clock Input Waveform

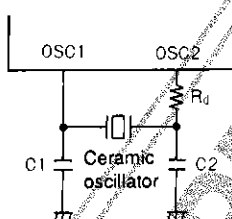


Figure 2: Ceramic Oscillator Circuit

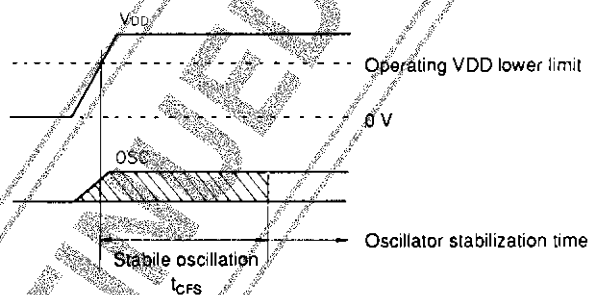


Figure 3: Oscillator Stabilization Time

Table 1: Ceramic Oscillator Guaranteed Constants

Capacitance: External	4 MHz (Murata, Ltd.) CSA4.00MG	C1 = 33 pF ±10%	4 MHz (Kyocera, Ltd.) KBR4.0MS	C1 = 33 pF ±10%
		C1 = 33 pF ±10%		C1 = 33 pF ±10%
		Rd = 0 Ω		Rd = 0 Ω
Capacitance: Internal	4 MHz (Murata, Ltd.) CST4.00MG		4 MHz (Kyocera, Ltd.) KBR4.0MES	

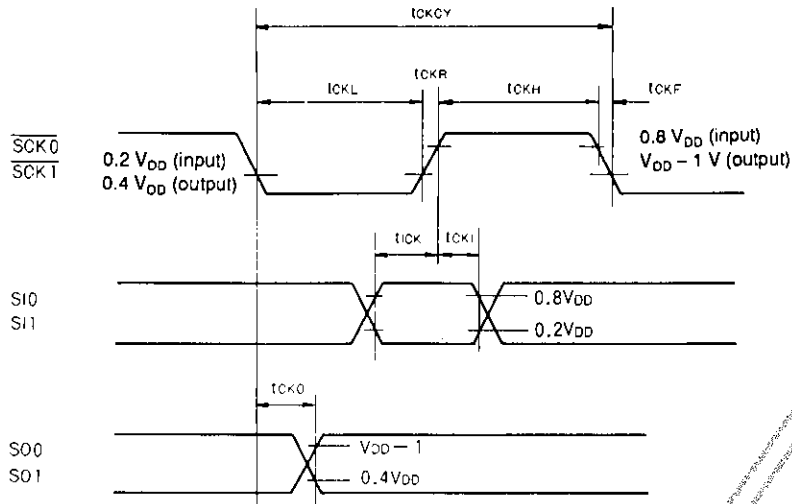


Figure 4: Serial I/O Timing

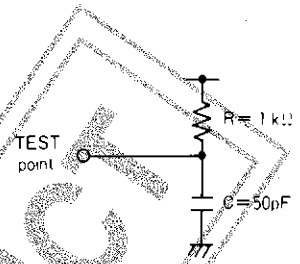


Figure 5: Timing Load

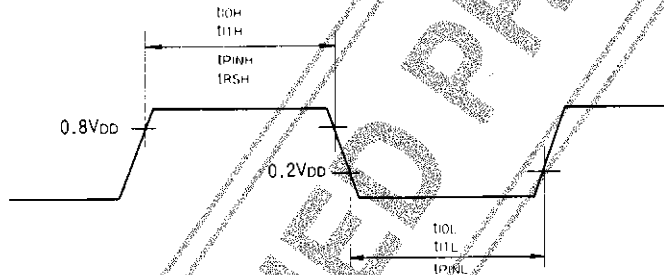


Figure 6: INT0, INT1, INT2, INT3, INT4, INT5, PIN1, and RES Input Timing

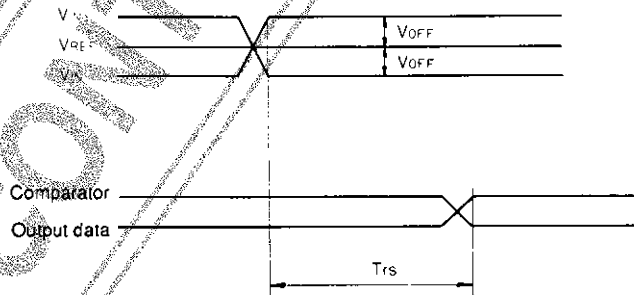
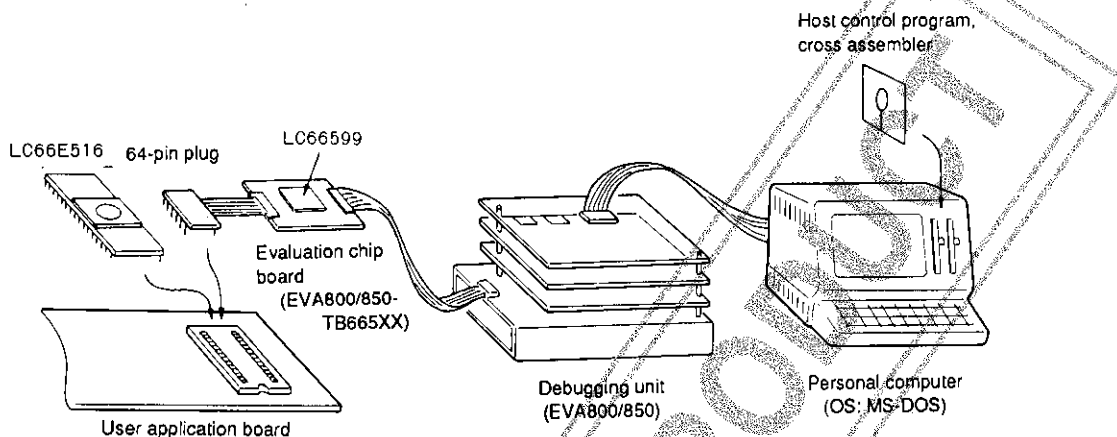


Figure 7: Timing of the Comparator Response Speed Trs

Application Development Tools

Program development for the LC66562B and LC66566B is performed on an IBM compatible PC running MS-DOS. A cross assembler is available for each product. In addition, to assist program development, a program debugging unit (EVA850/800), an evaluation chip board (EVA850/800-TB665XX), and evaluation chip (LC66599) and a built-in EPROM microcontroller (LC66E516) are available.



Structure of the Application Development Tools

1. Program Debugging Unit (EVA850/800)

This is an emulator that provides an EPROM writing function and a function for serial data communication with external equipment, such as the host computer. It supports machine language application development as well as program correction and debugging. It provides program breaking, stepping, and tracing as its main debugging functions. Note that the EVA850/800 monitor ROM uses the MPM665XX.

2. Evaluation chip board (EVA800/850-TB665XX)

The evaluation chip board takes the control signals and ports output by the evaluation chip to a 64-pin connector, and converts them to a pin layout identical to that of mass produced chips. The evaluation chip board has jumper cables for option and state settings that allow I/O formats and functions identical to the mass produced chip to be setup.

Note however that the hold mode clear timing, and certain electrical characteristics will differ.

Jumpers

Type	OSC		Reset method		User application board power supply technique	
Jumper name	Jumper 1 (J1)		Jumper 2 (J2: RES)		Jumper 3 (J3: V _{DD})	
Jumper setting and mode	EXT	External oscillator (external clock)	INT (a)	Reset on a RUN instruction from the host computer	ON (a)	Supply V _{DD} to the user application board over the evaluation chip board output
	RC	RC oscillator	EXT (b)	Reset using a reset circuit on the user application board	OFF (b)	Use separate power supplies for the user application board and the evaluation chip power supply
	CF	CF oscillator				

Switches (SW1)

Type	Port 0, 1, and 8 output level on reset						Watchdog timer setting	
	P0S		P1S		P8S		WDC	
Switch name	ON	Port 0 high	ON	Port 1 high	ON	Port 8 high	ON	Watchdog timer
Switch setting and mode	OFF	Port 0 low	OFF	Port 1 low	OFF	Port 8 low	OFF	No watchdog timer

Note: RC0 and RC1 must both be turned on.

Switches SW2 to SW14: Pull-up resistor option setting

- Set these switches to the on position for ports for which the pull-up resistor option is selected, and set them to the open position when the open drain option is specified. (SW10 — port 8 is for the pull-down resistor selection.)
- These can be set for individual port pins.

3. Cross Assembler

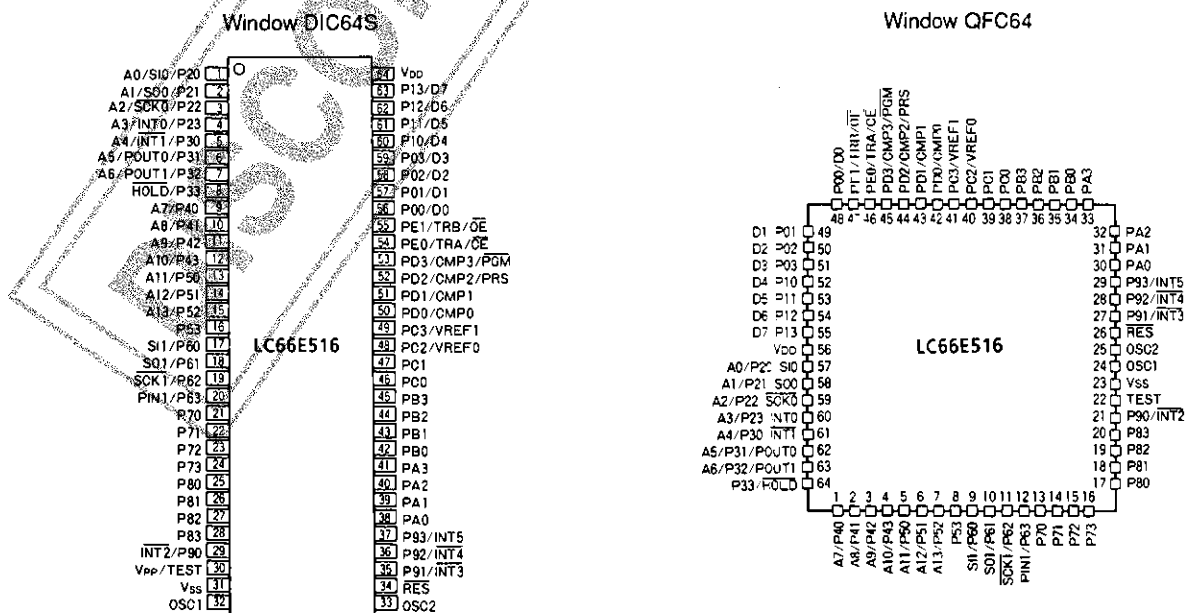
Cross assembler file name	Corresponding machine type	Programming limitations
LC66S. EXE	LC66562B/566B (LC66E516/P516) (LC66559)	4 SB instruction limitations • LC66562B: SB0, SB1, and SB2 can be used • LC66566B: SB0, SB1, SB2, and SB3 can be used • LC66E516/P516: SB0, SB1, SB2, and SB3 can be used • LC66559: SB0, SB1, SB2, and SB3 can be used

4. Simulation Chip (Refer to the LC66E516 Semiconductor Development News for details.)

The LC66E516 is a built-in EPROM microcontroller. By using a special purpose conversion board (the W66E516DH for DIP, and the W66E516QH for QFP versions) commercial PROM writers can be used to write programs. This allows the operation when mounted in an actual application to be confirmed.

- Form**
The LC66E516 has the same pin layout and functions as the LC66562B and LC66566B. Note however that the hold mode clear timing, and certain electrical characteristics will differ. The pin assignment is shown in the figures below.
- Options**
The options for the microcontroller to be evaluated (the port 0, 1, and 8 output levels after reset, the watchdog timer, and the port output formats) can be specified by setting internal EPROM data values. This allows evaluation using the same peripheral circuits as the end-product mass production board.

Pin Assignment



LC665XX Series Instruction Set Overview (by function)

Abbreviations used:

AC: Accumulator
 E: E register
 CF: Carry flag
 ZF: Zero flag
 HL: Data pointer DPH, DPL
 XY: Data pointer DPX, DPY
 M: Data memory
 M(HL): Data memory specified by the DPH, DPL data pointer
 M(XY): Data memory specified by the DPX, DPY auxiliary data pointer
 M2(HL): Two words of data memory (starting at an even address) specified by the DPH, DPL data pointer
 SP: Stack pointer
 M2(SP): Two words of data memory specified by the stack pointer
 M4(SP): Four words of data memory specified by the stack pointer
 in: N bits of immediate data
 t2: Bit specification

t2	11	10	01	00
Bit	2 ³	2 ²	2 ¹	2 ⁰

PCh: Bits 8 to 11 of the PC
 PCm: Bits 4 to 7 of the PC
 PCl: Bits 0 to 3 of the PC
 Fn: User flag, n = 0 to 15
 TIMER0: Timer 0
 TIMER1: Timer 1
 SIO: Serial I/O register
 P: Port
 P(i4): A port specified by 4 bits of immediate data
 INT: Interrupt flag
 (), []: Indicates content
 ←: Transfer direction, result
 ∨: Exclusive or
 ∧: Logical or
 ∨: Logical and
 +: Addition
 -: Subtraction
 —: Take the one's complement

LC66562B, 66566B

Instruction group	Mnemonic		Instruction code				Byte count	Cycle count	Operation	Description of operation	Status changes	Notes				
			D ₇	D ₆	D ₅	D ₄							D ₃	D ₂	D ₁	D ₀
Accumulator manipulation instructions	CLA	Clear AC	1	0	0	0	0	0	0	0	1	1	$AC \leftarrow 0$ (equivalent to LAI 0)	Clears AC	ZF	Also has a vertical skip function
	DAA	Decimal adjust AC in addition	1	1	0	0	0	0	1	0	2	2	$AC \leftarrow (AC) + 6$ (equivalent to ADI 6)	Adds 6 to AC	ZF	
	DAS	Decimal adjust AC in subtraction	1	1	0	0	0	0	1	0	2	2	$AC \leftarrow (AC) + 10$ (equivalent to ADI 0, 0AH)	Adds 10 to AC	ZF	
	CLC	Clear CF	0	0	0	1	1	1	1	1	1	1	$CF \leftarrow 0$	Clears CF	CF	
	STC	Set CF	0	0	0	1	1	1	1	1	1	1	$CF \leftarrow 1$	Sets CF	CF	
	CMA	Complement AC	0	0	0	1	1	0	0	0	1	1	$AC \leftarrow (\overline{AC})$	Takes the one's complement of AC	ZF	
	IA	Increment AC	0	0	0	1	0	1	0	0	1	1	$AC \leftarrow (AC) + 1$	Adds 1 to AC	ZF, CF	
	DA	Decrement AC	0	0	1	0	0	1	0	0	1	1	$AC \leftarrow (AC) - 1$	Subtracts 1 from AC	ZF, CF	
	RAR	Rotate AC right through CF	0	0	0	1	0	0	0	0	1	1	$AC_3 \leftarrow (CF),$ $AC_n \leftarrow (AC_{n+1}),$ $CF \leftarrow (AC_0)$	Shifts AC (including CF) right	CF	
	RAL	Rotate AC left through CF	0	0	0	0	0	0	0	1	1	1	$AC_0 \leftarrow (CF),$ $AC_n + 1 \leftarrow (AC_n),$ $CF \leftarrow (AC_3)$	Shifts AC (including CF) left	CF, ZF	
	TAE	Transfer AC to E	0	1	0	0	0	1	0	1	1	1	$E \leftarrow (AC)$	Transfers the contents of AC to E		
	TEA	Transfer E to AC	0	1	0	0	0	1	1	0	1	1	$AC \leftarrow (E)$	Transfers the contents of E to AC	ZF	
XAE	Exchange AC with E	0	1	0	0	0	1	0	0	1	1	$(AC) \leftrightarrow (E)$	Exchanges the contents of AC and E			
Memory manipulation instructions	IM	Increment M	0	0	0	1	0	0	1	0	1	1	$M(HL) \leftarrow M(HL) + 1$	Adds 1 to M(HL)	ZF, CF	
	DM	Decrement M	0	0	1	0	0	0	1	0	1	1	$M(HL) \leftarrow M(HL) - 1$	Subtracts 1 from M(HL)	ZF, CF	
	IMDR i8	Increment M direct	1	1	0	0	0	1	1	1	2	2	$M(i8) \leftarrow M(i8) + 1$	Adds 1 to M(i8)	ZF, CF	
	DMDR i8	Decrement M direct	1	1	0	0	0	0	1	1	2	2	$M(i8) \leftarrow M(i8) - 1$	Subtracts 1 from M(i8)	ZF, CF	
	SMB i2	Set M data bit	0	0	0	0	1	1	i_1	i_0	1	1	$[M(HL), i2] \leftarrow 1$	Sets the bit in M(HL) specified by i_1/i_0		
	RMB i2	Reset M data bit	0	0	1	0	1	1	i_1	i_0	1	1	$[M(HL), i2] \leftarrow 0$	Clears the bit in M(HL) specified by i_1/i_0	ZF	
Arithmetic and comparison instructions	AD	Add M to AC	0	0	0	0	0	1	1	0	1	1	$AC \leftarrow (AC) + M(HL)$	Adds (two's complement) AC and the contents of M(HL) and stores the result in AC	ZF, CF	
	ADDR i8	Add M direct to AC	1	1	0	0	0	1	0	1	2	2	$AC \leftarrow (AC) + M(i8)$	Adds (two's complement) AC and the contents of M(i8) and stores the result in AC	ZF, CF	
	ADC	Add M to AC with CF	0	0	0	0	0	0	1	0	1	1	$AC \leftarrow (AC) + M(HL) + (CF)$	Adds (two's complement) the contents of AC, M(HL), and CF and stores the result in AC	ZF, CF	
	ADI i4	Add immediate data to AC	1	1	0	0	0	0	1	1	2	2	$AC \leftarrow (AC) + i_3, i_2, i_1, i_0$	Adds (two's complement) AC and the immediate data and stores the result in AC	ZF	
	SUBC	Subtract AC from M with CF	0	0	0	1	0	1	1	1	1	1	$AC \leftarrow [M(HL)] (AC) (CF)$	Subtracts (two's complement) AC and CF from the contents of M(HL) and stores the result in AC	ZF, CF	Set CF to 0 when there is a borrow, and to 1 when no borrow
	ANDA	And M with AC then store AC	0	0	0	0	0	1	1	1	1	1	$AC \leftarrow (AC) [M(HL)]$	Takes the logical and of AC and the contents of M(HL) and stores the result in AC	ZF	
	ORA	Or M with AC then store AC	0	0	0	0	0	1	0	1	1	1	$AC \leftarrow (AC) [M(HL)]$	Takes the logical or of AC and the contents of M(HL) and stores the result in AC	ZF	
	EXL	Exclusive or M with AC then store AC	0	0	0	1	0	1	0	1	1	1	$AC \leftarrow (AC) \vee [M(HL)]$	Takes the logical exclusive or of AC and the contents of M(HL) and stores the result in AC	ZF	
	ANDM	And M with AC then store M	0	0	0	0	0	0	1	1	1	1	$M(HL) \leftarrow (AC) [M(HL)]$	Takes the logical and of AC and the contents of M(HL) and stores the result in M(HL)	ZF	
ORM	Or M with AC then store M	0	0	0	0	0	1	0	0	1	1	$M(HL) \leftarrow (AC) [M(HL)]$	Takes the logical or of AC and the contents of M(HL) and stores the result in M(HL)	ZF		

Instruction group	Mnemonic	Instruction code								Byte count	Cycle count	Operation	Description of operation	Status changes	Notes													
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																			
Arithmetic and comparison instructions	CM	Compare AC with M	0	0	0	1	0	1	1	0	1	1	$[M(HL)] + (AC) + 1$	Compares the contents of AC and M(HL), and sets or resets the CF and ZF flags accordingly <table border="1"> <tr> <th>Magnitude relationship</th> <th>CF</th> <th>ZF</th> </tr> <tr> <td>$[M(HL)] > (AC)$</td> <td>0</td> <td>0</td> </tr> <tr> <td>$[M(HL)] = (AC)$</td> <td>1</td> <td>1</td> </tr> <tr> <td>$[M(HL)] < (AC)$</td> <td>1</td> <td>0</td> </tr> </table>	Magnitude relationship	CF	ZF	$[M(HL)] > (AC)$	0	0	$[M(HL)] = (AC)$	1	1	$[M(HL)] < (AC)$	1	0	ZF, CF	
	Magnitude relationship	CF	ZF																									
	$[M(HL)] > (AC)$	0	0																									
	$[M(HL)] = (AC)$	1	1																									
$[M(HL)] < (AC)$	1	0																										
CI i4	Compare AC with immediate data	1	1	0	0	1	1	1	1	2	2	$[i_3 i_2 i_1 i_0] + (AC) + 1$	Compares the contents of AC with the immediate data $i_3 i_2 i_1 i_0$ and sets or resets the CF and ZF flags accordingly <table border="1"> <tr> <th>Magnitude relationship</th> <th>CF</th> <th>ZF</th> </tr> <tr> <td>$i_3 i_2 i_1 i_0 > AC$</td> <td>0</td> <td>0</td> </tr> <tr> <td>$i_3 i_2 i_1 i_0 = AC$</td> <td>1</td> <td>1</td> </tr> <tr> <td>$i_3 i_2 i_1 i_0 < AC$</td> <td>1</td> <td>0</td> </tr> </table>	Magnitude relationship	CF	ZF	$i_3 i_2 i_1 i_0 > AC$	0	0	$i_3 i_2 i_1 i_0 = AC$	1	1	$i_3 i_2 i_1 i_0 < AC$	1	0	ZF, CF		
Magnitude relationship	CF	ZF																										
$i_3 i_2 i_1 i_0 > AC$	0	0																										
$i_3 i_2 i_1 i_0 = AC$	1	1																										
$i_3 i_2 i_1 i_0 < AC$	1	0																										
CLI i4	Compare DP _L with immediate data	1	1	0	0	1	1	1	1	2	2	$ZF \leftarrow 1$ if $(DP_L) = i_3 i_2 i_1 i_0$ $ZF \leftarrow 0$ if $(DP_L) \neq i_3 i_2 i_1 i_0$	Compares DP _L with the immediate data, and either sets ZF if they were equal or clears ZF if different	ZF														
CMB i2	Compare AC bit with M data bit	1	1	0	0	1	1	1	1	2	2	$ZF \leftarrow 1$ if $(AC, i_2) = (M(HL), i_2)$ $ZF \leftarrow 0$ if $(AC, i_2) \neq (M(HL), i_2)$	Compares the bit specified by the two bits $i_1 i_0$ in the contents of AC and M(HL), and either sets ZF if they were equal or clears ZF if different	ZF														
Load and store instructions	LAE	Load AC and E from M2(HL)	0	1	0	1	1	1	0	0	1	1	$AC \leftarrow M(HL)$ $E \leftarrow M(HL + 1)$	Loads the contents of M2(HL) into AC and E														
	LAI i4	Load AC with immediate data	1	0	0	0	i_3	i_2	i_1	i_0	1	1	$AC \leftarrow i_3 i_2 i_1 i_0$	Loads immediate data into AC	ZF	Also has a vertical skip function												
	LADR i8	Load AC from M direct	1	1	0	0	i_7	i_6	i_5	i_4	2	2	$AC \leftarrow [M(i_8)]$	Loads the contents of M(i8) into AC	ZF													
	S	Store AC to M	0	1	0	0	0	1	1	1	1	1	$M(HL) \leftarrow (AC)$	Stores the contents of AC into M(HL)														
	SAE	Store AC and E to M2(HL)	0	1	0	1	1	1	1	0	1	1	$M(HL) \leftarrow (AC)$ $M(HL + 1) \leftarrow (E)$	Stores the contents of AC and E into M2(HL)														
	LA reg	Load AC from M(reg)	0	1	0	0	1	0	i_0	0	1	1	$AC \leftarrow [M(reg)]$	Loads the contents of M(reg) into AC. reg is either HL or XY.	ZF													
	LA reg, i	Load AC from M(reg) then increment reg	0	1	0	0	1	0	i_0	1	1	2	$AC \leftarrow [M(reg)]$ $DP_L \leftarrow (DP_L) + 1$ Or: $DP_Y \leftarrow (DP_Y) + 1$	Loads the contents of M(reg) into AC. reg is either HL or XY. Then, it increments either DP _L or DP _Y . The relationship between reg and i_0 is the same as that for LA reg.	ZF	ZF is set according to the result of the increment of DP _L or DP _Y												
	LA reg, D	Load AC from M(reg) then decrement reg	0	1	0	1	1	0	i_0	1	1	2	$AC \leftarrow [M(reg)]$ $DP_L \leftarrow (DP_L) - 1$ Or: $DP_Y \leftarrow (DP_Y) - 1$	Loads the contents of M(reg) into AC. reg is either HL or XY. Then, it decrements either DP _L or DP _Y . The relationship between reg and i_0 is the same as that for XA reg.	ZF	ZF is set according to the result of the increment of DP _L or DP _Y												
XA reg	Exchange AC with M(reg)	0	1	0	0	1	1	i_0	0	1	1	$(AC) \leftrightarrow [M(reg)]$	Exchanges the contents of M(reg) and AC. reg is either HL or XY.															

LC66562B, 66566B

Instruction group	Mnemonic	Instruction code								Byte count	Cycle count	Operation	Description of operation	Status changes	Notes					
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀											
Load and store instructions	XA reg. I	Exchange AC with M(reg) then increment reg	0	1	0	0	1	1	1	0	1	1	2	(AC) \leftrightarrow [M(reg)] DP _L \leftarrow (DP _L) + 1 Or: DP _V \leftarrow (DP _V) + 1	Exchanges the contents of M(reg) and AC. reg is either HL or XY. Then, it increments either DP _L or DP _V . The relationship between reg and I ₀ is the same as that for XA-reg	ZF	ZF is set according to the result of the increment of DP _L or DP _V			
	XA reg. D	Exchange AC with M(reg) then decrement reg	0	1	0	1	1	1	1	0	1	1	2	(AC) \leftrightarrow [M(reg)] DP _L \leftarrow (DP _L) - 1 Or: DP _V \leftarrow (DP _V) - 1	Exchanges the contents of M(reg) and AC. reg is either HL or XY. Then, it decrements either DP _L or DP _V . The relationship between reg and I ₀ is the same as that for XA-reg	ZF	ZF is set according to the result of the increment of DP _L or DP _V			
	XADR i8	Exchange AC with M direct	1	1	0	0	1	0	0	0	1	0	2	2	(AC) \leftrightarrow [M(i8)]	Exchanges the contents of AC and M(i8)				
	LEAI i8	Load E and AC with immediate data	1	1	0	0	0	1	1	0	1	0	2	2	E \leftarrow I ₇ I ₆ I ₅ I ₄ AC \leftarrow I ₃ I ₂ I ₁ I ₀	Loads the immediate data i8 into E and AC				
	RTBL	Read table data from program ROM	0	1	0	1	1	0	1	0	1	0	1	2	E, AC \leftarrow [ROM(PCh, E, AC)]	Loads into E and AC the ROM data at the location specified by the PC with the lower 8 bits replaced by the contents of E and AC				
	RTBLP	Read table data from program ROM then output to P4, 5	0	1	0	1	1	0	0	0	1	0	1	2	Port 4, 5 \leftarrow [ROM(PCh, E, AC)]	Outputs to ports 4 and 5 the ROM data at the location specified by the PC with the lower 8 bits replaced by the contents of E and AC				
Data and pointer manipulation instructions	LDZ i4	Load DP _H with zero and DP _L with immediate data respectively	0	1	1	0	I ₃	I ₂	I ₁	I ₀	1	1	1	1	DP _H \leftarrow 0 DP _L \leftarrow I ₃ I ₂ I ₁ I ₀	Loads zero into DP _H and the immediate data i4 into DP _L				
	LHI i4	Load DP _H with immediate data	1	1	0	0	0	0	0	0	I ₃	I ₂	I ₁	I ₀	2	2	DP _H \leftarrow I ₃ I ₂ I ₁ I ₀	Loads the immediate data i4 into DP _H		
	LLI i4	Load DP _L with immediate data	1	1	0	0	0	0	0	1	I ₃	I ₂	I ₁	I ₀	2	2	DP _L \leftarrow I ₃ I ₂ I ₁ I ₀	Loads the immediate data i4 into DP _L		
	LHLI i8	Load DP _H , DP _L with immediate data	1	1	0	0	0	0	0	0	I ₃	I ₂	I ₁	I ₀	2	2	DP _H \leftarrow I ₇ I ₆ I ₅ I ₄ DP _L \leftarrow I ₃ I ₂ I ₁ I ₀	Loads immediate data into DP _H and DP _L		
	LXYI i8	Load DP _X , DP _Y with immediate data	1	1	0	0	0	0	1	0	I ₃	I ₂	I ₁	I ₀	2	2	DP _X \leftarrow I ₇ I ₆ I ₅ I ₄ DP _Y \leftarrow I ₃ I ₂ I ₁ I ₀	Loads immediate data into DP _X and DP _Y		
	IL	Increment DP _L	0	0	0	1	0	0	0	1	0	0	0	1	1	1	DP _L \leftarrow (DP _L) + 1	Increments the contents of DP _L	ZF	
	DL	Decrement DP _L	0	0	1	0	0	0	0	1	0	0	0	1	1	1	DP _L \leftarrow (DP _L) - 1	Decrements the contents of DP _L	ZF	
	IY	Increment DP _Y	0	0	0	1	0	0	1	1	0	0	1	1	1	1	DP _Y \leftarrow (DP _Y) + 1	Increments the contents of DP _Y	ZF	
	DY	Decrement DP _Y	0	0	1	0	0	0	1	1	0	0	1	1	1	1	DP _Y \leftarrow (DP _Y) - 1	Decrements the contents of DP _Y	ZF	
	TAH	Transfer AC to DP _H	1	1	0	0	1	1	1	1	0	0	0	0	2	2	DP _H \leftarrow (AC)	Transfers the contents of AC into DP _H		
	THA	Transfer DP _H to AC	1	1	0	0	1	1	1	1	0	0	0	0	2	2	AC \leftarrow (DP _H)	Transfers the contents of DP _H into AC	ZF	
	XAH	Exchange AC with DP _H	0	1	0	0	0	0	0	0	0	0	0	0	1	1	(AC) \leftrightarrow (DP _H)	Exchanges the contents of AC and DP _H		
	TAL	Transfer AC to DP _L	1	1	0	0	1	1	1	1	0	0	0	1	2	2	DP _L \leftarrow (AC)	Transfers the contents of AC into DP _L		
	TLA	Transfer DP _L to AC	1	1	0	0	1	1	1	1	0	0	0	1	2	2	AC \leftarrow (DP _L)	Transfers the contents of DP _L into AC	ZF	
	XAL	Exchange AC with DP _L	0	1	0	0	0	0	0	1	0	0	0	1	1	1	(AC) \leftrightarrow (DP _L)	Exchanges the contents of AC and DP _L		
	TAX	Transfer AC to DP _X	1	1	0	0	1	1	1	1	0	0	1	0	2	2	DP _X \leftarrow (AC)	Transfers the contents of AC into DP _X		
	TXA	Transfer DP _X to AC	1	1	0	0	1	1	1	1	0	0	1	0	2	2	AC \leftarrow (DP _X)	Transfers the contents of DP _X into AC	ZF	
	XAX	Exchange AC with DP _X	0	1	0	0	0	0	1	0	0	0	1	0	1	1	(AC) \leftrightarrow (DP _X)	Exchanges the contents of AC and DP _X		
TAY	Transfer AC to DP _Y	1	1	0	0	1	1	1	1	0	0	1	1	2	2	DP _Y \leftarrow (AC)	Transfers the contents of AC into DP _Y			
TYA	Transfer DP _Y to AC	1	1	0	0	1	1	1	1	0	0	1	1	2	2	AC \leftarrow (DP _Y)	Transfers the contents of DP _Y into AC	ZF		
XAY	Exchange AC with DP _Y	0	1	0	0	0	0	1	1	0	0	1	1	1	1	(AC) \leftrightarrow (DP _Y)	Exchanges the contents of AC and DP _Y			

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Instruction group	Mnemonic	Instruction code								Byte count	Cycle count	Operation	Description of operation	Status changes	Notes
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀						
Branch instructions	BPI2 addr	Branch on port bit	1 1 0 1	1 0 1 0	P ₇ P ₆ P ₅ P ₄	P ₃ P ₂ P ₁ P ₀	2	2	PC7 to PC0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DP _J), i2) = 1	Branches to the location specified by P ₇ to P ₀ on the current page if the port (DP _J) bit specified by the immediate data i ₁ /i ₀ is 1		Also valid for internal control registers by use directly following a bank instruction. However, this is limited to registers that allow reads.			
	BNPI2 addr	Branch on no port bit	1 0 0 1	1 0 1 0	P ₇ P ₆ P ₅ P ₄	P ₃ P ₂ P ₁ P ₀	2	2	PC7 to PC0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (P(DP _J), i2) = 0	Branches to the location specified by P ₇ to P ₀ on the current page if the port (DP _J) bit specified by the immediate data i ₁ /i ₀ is 0		Also valid for internal control registers by use directly following a bank instruction. However, this is limited to registers that allow reads.			
	BC addr	Branch on CF	1 1 0 1	1 1 0 0	P ₇ P ₆ P ₅ P ₄	P ₃ P ₂ P ₁ P ₀	2	2	PC7 to PC0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (CF) = 1	Branches to the location specified by P ₇ to P ₀ on the current page if CF is 1					
	BNC addr	Branch on no CF	1 0 0 1	1 1 0 0	P ₇ P ₆ P ₅ P ₄	P ₃ P ₂ P ₁ P ₀	2	2	PC7 to PC0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (CF) = 0	Branches to the location specified by P ₇ to P ₀ on the current page if CF is 0					
	BZ addr	Branch on ZF	1 1 0 1	1 1 0 1	P ₇ P ₆ P ₅ P ₄	P ₃ P ₂ P ₁ P ₀	2	2	PC7 to PC0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (ZF) = 1	Branches to the location specified by P ₇ to P ₀ on the current page if ZF is 1					
	BNZ addr	Branch on no ZF	1 0 0 1	1 1 0 1	P ₇ P ₆ P ₅ P ₄	P ₃ P ₂ P ₁ P ₀	2	2	PC7 to PC0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (ZF) = 0	Branches to the location specified by P ₇ to P ₀ on the current page if ZF is 0					
	BFn4 addr	Branch on flag bit	1 1 1 1	n ₃ n ₂ n ₁ n ₀	P ₇ P ₆ P ₅ P ₄	P ₃ P ₂ P ₁ P ₀	2	2	PC7 to PC0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (Fn) = 1	Branches to the location specified by P ₇ to P ₀ on the current page if, of the 16 flags, the flag specified by n ₃ to n ₀ is 1					
	BNFn4 addr	Branch on no flag bit	1 0 1 1	n ₃ n ₂ n ₁ n ₀	P ₇ P ₆ P ₅ P ₄	P ₃ P ₂ P ₁ P ₀	2	2	PC7 to PC0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if (Fn) = 0	Branches to the location specified by P ₇ to P ₀ on the current page if, of the 16 flags, the flag specified by n ₃ to n ₀ is 0					
I/O instructions	IP0	Input port 0 to AC	0 0 1 0	0 0 0 0			1	1	AC ← (P0)	Inputs the contents of port 0 to AC	ZF				
	IP	Input port to AC	0 0 1 0	0 1 1 0			1	1	AC ← [P(DP _J)]	Inputs the contents of port P(DP _J) to AC	ZF				
	IPM	Input port to M	0 0 0 1	1 0 0 1			1	1	M(HL) ← [P(DP _J)]	Inputs the contents of port P(DP _J) to M(HL)					
	IPDR i4	Input port to AC direct	1 1 0 0	1 1 1 1			2	2	AC ← [P(i4)]	Inputs the contents of port P(i4) to AC	ZF				
	IP45	Input port 4-5 to E, AC respectively	1 1 0 0	1 1 1 1			2	2	E ← [P(4)] AC ← [P(5)]	Inputs the contents of ports P(4) and P(5) to E and AC, respectively					
	OP	Output AC to port	0 0 1 0	0 1 0 1			1	1	P(DP _J) ← (AC)	Outputs the contents of AC to port P(DP _J)					
	OPM	Output M to port	0 0 0 1	1 0 1 0			1	1	P(DP _J) ← [M(HL)]	Outputs the contents of M(HL) to port P(DP _J)					
	OPDR i4	Output AC to port direct	1 1 0 0	1 1 1 1			2	2	P(i4) ← (AC)	Outputs the contents of AC to port P(i4)					
	OP45	Output E, AC to port 4, 5 respectively	1 1 0 0	1 1 1 1			2	2	P(4) ← (E) P(5) ← (AC)	Outputs the contents of E and AC to ports P(4) and P(5), respectively					
	SPB i2	Set port bit	0 0 0 0	1 0 1 0			1	1	[P(DP _J), i2] ← 1	Sets the port P(DP _J) bit specified by the immediate data i ₁ /i ₀					
RPB i2	Reset port bit	0 0 1 0	1 0 1 0			1	1	[P(DP _J), i2] ← 0	Clears the port P(DP _J) bit specified by the immediate data i ₁ /i ₀	ZF					

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Instruction group	Mnemonic	Instruction code								Byte count	Cycle count	Operation	Description of operation	Status changes	Notes
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀						
I/O instructions	ANDPDR i4, p4	1 1 0 0 0 1 0 1 i ₃ i ₂ i ₁ i ₀ P ₃ P ₂ P ₁ P ₀								2	2	$P(P_3 \text{ to } P_0) \leftarrow [P(P_3 \text{ to } P_0)] \vee i_3 \text{ to } i_0$	Outputs to port P(P ₃ to P ₀) the result of taking the logical and of port P(P ₃ to P ₀) and the immediate data i ₃ to i ₀	ZF	
	ORPDR i4, p4	1 1 0 0 0 1 0 0 i ₃ i ₂ i ₁ i ₀ P ₃ P ₂ P ₁ P ₀								2	2	$P(P_3 \text{ to } P_0) \leftarrow [P(P_3 \text{ to } P_0)] \vee i_3 \text{ to } i_0$	Outputs to port P(P ₃ to P ₀) the result of taking the logical or of port P(P ₃ to P ₀) and the immediate data i ₃ to i ₀	ZF	
Timer control instructions	WTTM0	1 1 0 0 1 0 1 0								1	2	TIMER0 ← (M2(HL), AC)	Writes the contents of M2(HL) and AC into the timer 0 reload register		
	WTTM1	1 1 0 0 1 1 1 1 1 1 1 1 0 1 0 0								2	2	TIMER1 ← (E), (AC)	Writes the contents of E and AC into the timer 1 reload register A		
	RTIM0	1 1 0 0 1 0 1 1								1	2	M2(HL), AC ← (TIMER0)	Reads out the contents of the timer 0 counter into M2(HL) and AC		
	RTIM1	1 1 0 0 1 1 1 1 1 1 1 1 0 1 0 1								2	2	E, AC ← (TIMER1)	Reads out the contents of the timer 1 counter into E and AC		
	START0	1 1 0 0 1 1 1 1 1 1 1 0 0 1 1 0								2	2	Start timer 0 counter	Starts the timer 0 counter		
	START1	1 1 0 0 1 1 1 1 1 1 1 0 0 1 1 1								2	2	Start timer 1 counter	Starts the timer 1 counter		
	STOP0	1 1 0 0 1 1 1 1 1 1 1 1 0 1 1 0								2	2	Stop timer 0 counter	Stops the timer 0 counter		
	STOP1	1 1 0 0 1 1 1 1 1 1 1 1 0 1 1 1								2	2	Stop timer 1 counter	Stops the timer 1 counter		
Interrupt control instructions	MSET	1 1 0 0 1 1 0 1 0 1 0 1 0 0 0 0								2	2	MSE ← 1	Sets the interrupt master enable flag		
	MRESET	1 1 0 0 1 1 0 1 1 0 0 1 0 0 0 0								2	2	MSE ← 0	Clears the interrupt master enable flag		
	EIH i4	1 1 0 0 1 1 0 1 0 1 0 1 i ₃ i ₂ i ₁ i ₀								2	2	EDIH ← (EDIH) ∨ i4	Sets the interrupt enable flags		
	EIL i4	1 1 0 0 1 1 0 1 0 1 0 0 i ₃ i ₂ i ₁ i ₀								2	2	EDIL ← (EDIL) ∨ i4	Sets the interrupt enable flags		
	DIH i4	1 1 0 0 1 1 0 1 1 0 0 1 i ₃ i ₂ i ₁ i ₀								2	2	EDIH ← (EDIH) ∧ i4	Clears the interrupt enable flags	ZF	
	DIL i4	1 1 0 0 1 1 0 1 1 0 0 0 i ₃ i ₂ i ₁ i ₀								2	2	EDIL ← (EDIL) ∧ i4	Clears the interrupt enable flags	ZF	
	WTSP	1 1 0 0 1 1 1 1 1 1 0 1 1 0 1 0								2	2	SP ← (E), (AC)	Transfer the contents of E and AC into SP		
RSP	1 1 0 0 1 1 1 1 1 1 0 1 1 0 1 1								2	2	E, AC ← (SP)	Transfers the contents of SP into E and AC			
Standby control instructions	HALT	1 1 0 0 1 1 1 1 1 1 0 1 1 1 1 0								2	2	HALT	Sets halt mode		
	HOLD	1 1 0 0 1 1 1 1 1 1 0 1 1 1 1 1								2	2	HOLD	Sets hold mode		
Serial I/O control instructions	STARTS	1 1 0 0 1 1 1 1 1 1 1 0 1 1 1 0								2	2	START SIO	Starts SIO operation		
	WTSIO	1 1 0 0 1 1 1 1 1 1 0 1 1 1 1 1								2	2	SIO ← (E), (AC)	Writes the contents of E and AC into the SIO register		
	RSIO	1 1 0 0 1 1 1 1 1 1 1 1 1 1 1 1								2	2	E, AC ← (SIO)	Reads the contents of the SIO register into E and AC		
Other instructions	NOP	0 0 0 0 0 0 0 0								1	1	No operation	Takes up a single machine cycle without performing an operation		
	SB i2	1 1 0 0 1 1 1 1 1 1 0 0 0 0 i ₁ i ₀								2	2	PC13, 12 ← i ₁ i ₀	Specifies the memory bank		

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